Clock Gating Aware Low Power ALU Design and Implementation on FPGA

Bishwajeet Pandey and Manisha Pattanaik

***Abstract*—This paper deals with the design and implementation of a Clock Gating Aware Low Power Arithmetic and Logic Unit that has been developed as part of low power processor design in the platform Xilinx ISE 14.2 and synthesized on 90nm Spartan-3 FPGA. Clock power contributes 45-60 percent of total dynamic power. Hence, clock power reduction is necessary in low power design. In this paper, we analyze theoretical 93.75% clock power reduction in ALU using clock gating techniques. On simulator, we achieved 88.23% clock power reduction using latch based clock gating and 70.58% clock power reduction using latch free clock gating.**

***Index Terms*—Clock gate, ALU, FPGA, LUT, clock power, register transfer level, dynamic power, leakage power**

I. Introduction

Low Power ALU Design is based on application of clock gate to turn off the sub-module of ALU that is not in use by current executing instruction as decided by instruction decoder unit. According to [1]-[3], Clock Power consumes 50-70 percent of total chip power and will increase in the next coming generation of hardware designs at 32nm and below. Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by hardware designers and is typically implemented by RTL-level HDL Simulator or gate level power analyser tools.

$$Power = C_L \times (Voltage) \times (frequency)$$

In equation (1) power is directly proportional to the square of voltage and the frequency of the clock.

A. Statement of the Problem:

Clock gating is used in VLSI circuit design to reduce dynamic power by gating off the functional unit that is not in use by current executing instructions as decided by instruction decoder unit.

II. Literature Review

Clock Enable consumed More Power and Clock Gating consumed Less Power [1]. According to reference [2], Power optimization, traditionally relegated to the synthesis and circuits level, now shifted to the System Level and Register-Transfer-Level. This is possible due to clock gating which switch off the inactive units of the design and reduce overall power consumption. There are many clock gating styles available to optimize power in VLSI circuits. They can be:

- Latch-free based CG design.
- Latch-based CG design.
- Flip-flop based CG design.
- Intelligent CG design.

A. Latch-free Clock Gated ALU design

We use an AND gate in clock gate if clock is active on the rising edge. We use an OR gate in clock gate if clock is active on the falling edge. Using idea given in [2] and [4], we develop following ALU design as shown in Fig. 1.

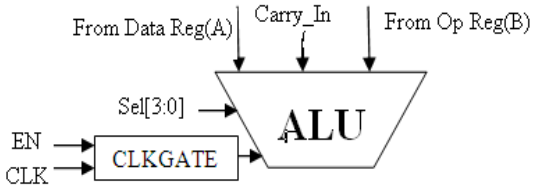

Fig. 1. Latch free clock gated design

B. Problem in Latch-Free Clock Gated Design

If enable signal goes inactive in between the clock pulse then gated clock terminated before his life time as shown in Fig. 2.

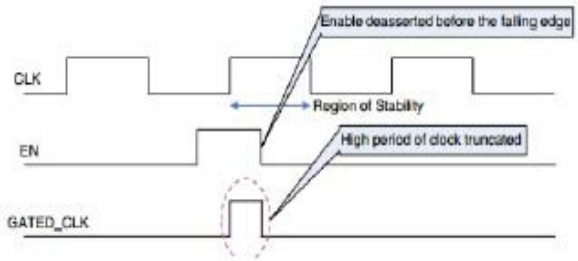

Fig. 2. Problem in latch-free clock gated design

C. Latch Based Clock Gated ALU Design

The latch-based clock gate consists of a level sensitive latch in design to hold the enable signal from the active edge to the inactive edge of the clock as shown in Fig. 3.

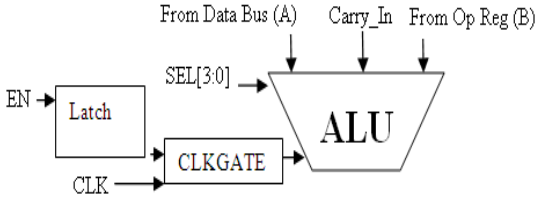

Fig. 3. Latch based clock gated ALU design

D. Flip-Flop Based Clock gated ALU Design

The Flip-Flop based clock gate consists of a level sensitive latch in design to hold the enable signal from the active edge

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to the inactive edge of the clock as shown in Fig. 4.

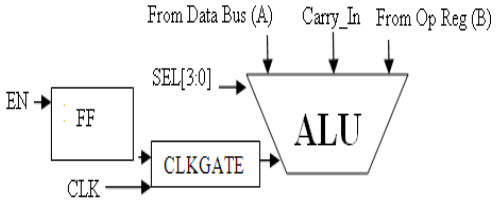

Fig. 4. Flip-flop based clock gated ALU design

Reference [5] presents the design and implementation of a self-timed arithmetic logic unit (ALU) that has been developed as part of an asynchronous microprocessor. Reference [5] displays an inherent operational characteristic of low consumption, owing to the synchronization signals that stop when the execution of an operation finishes (stoppable clock); that is a precursor of clock gating. Our whole work of clock gating is an extension of the work done in [5] i.e. switch off functional unit when unit is not in use. ALU in [6] performs 16 instructions and has a two-stage pipelined architecture. For low power consumption, [6] propose a new ALU architecture which has an efficient ELM adder of propagation (P) and generation (G) block scheme. The operation of an adder of the proposed ALU is disabled while the logical operation is performed and vice versa, this concept is same as our clock gating approach, here we also switching off the arithmetic function when logical function in use and vice versa using clock gate approach. In outputs of [6], P block are separated to become dual bus to reduce switching capacitances during the ALU operation.

TABLE I: FUNCTION OF ALU

Functions of Arithmetic and Logic Unit			
Unary	**Sel**	**Arithmetic & Logic**	**Sel**
Clear	0000	Add	1000
Hold B	0001	Subtract	1001
Complement B	0010	Add Carry	1010
Hold A	0011	Subtract Borrow	1011
Complement A	0100	Logical AND	1100
Decrement A	0101	Logical OR	1101
Increment A	0110	Logical XOR	1110
Shift Left A	0111	Logical XNOR	1111
All Flags are unaffected in execution of Unary except Carry Flag in Shift		All Flag set in every operation from 1000-1111.	

III. INTRODUCTION OF CLOCK GATED ALU

A, B are the two input buses and carry in, Sel [3:0], CLK are others input. Output bus ALU Out returns the result of the ALU operation. OC [7:4] portmap to Sel [3:0] determines which operation is performed as shown in Fig. 5.

A. Operations Performed in ALU

Opcode of Size 4 i.e. OC [4:7] is portmap to Sel [3:0] to decode all instruction ranges from 0000-1111. Whereas first eight are unary function, next four are arithmetic function and last four are logic function. All function listed in Table1.

The ALU generates 4 flags-Zero (Z), Carry (C), Sign (S), and Parity (P). Flags are not affected by the Unary Logic functions. Only the C flag is affected by the Shift function. All flags are affected by the other ALU functions.

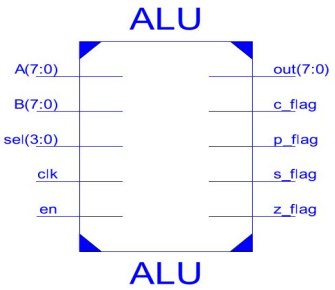

Fig. 5. Arithmetic and logic unit

IV. METHODOLOGY

A. Clear Function of ALU

The clear function reset the output of ALU to 8'h00. If we add clock gate in place of de-multiplexing clock signal to all 16 sub-modules of ALU then we reduce 93.75% power reduction as shown in Fig. 6 (a-b).

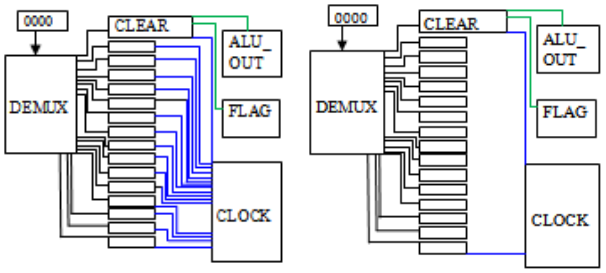

Fig. 6. Without clock gate (a), With clock gate (b)

B. Save Operand Register Value in ALU

Pass value of B to ALU output. ALU_Out=B; In Clock Gating, we turn off the supply of clock signal to rest 15 modules other than Save B. Hence reduce 93.75% power reduction as shown in Fig.7 (a-b).

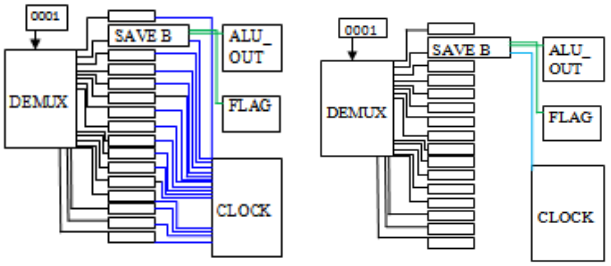

Fig. 7. Without clock gate (a), With clock gate (b)

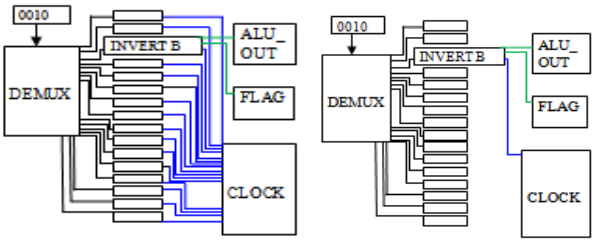

Fig. 8. Without CLOCK Gate (a), With clock gate (b)

C. Invert Operand Register Value in ALU

ALU out= ~B; Pass complemented value of B to ALU

output and not consider value of A. In Clock Gating, we turn off the 15 functional units as shown in Fig. 8. Hence reduce 93.75% power reduction.

D. Hold Data Bus Value

ALU out=A; Pass value of A to ALU output. In Clock Gating, we turn off the 15 functional units as shown in Fig. 9 Hence reduce 93.75% power reduction.

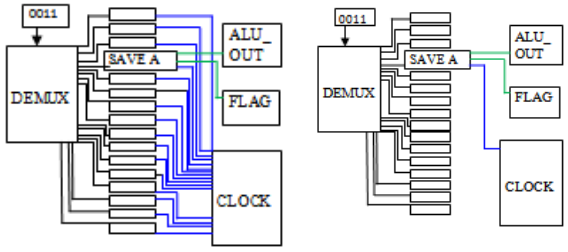

Fig. 9. Without Clock Gate (a), With Clock Gate (b)

E. Invert Data Bus Value

ALU out=_ A; Pass inverted value of A to ALU output. In Clock Gating, we turn off the 15 functional units as shown in Fig. 10. Hence reduce 93.75% power reduction.

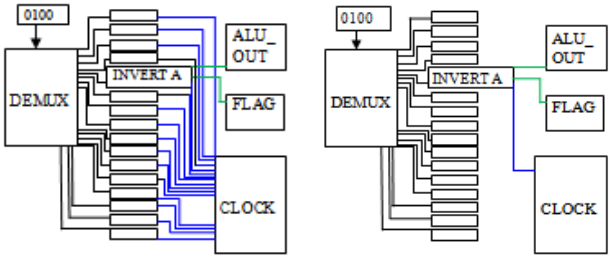

Fig. 10. Without Clock Gate (a), With Clock Gate (b)

F. Decrement Data Bus Value

ALU out=A-1; Pass decremented value of A to ALU output. In Clock Gating, we turn off the 15 functional units as shown in Fig. 11. Hence reduce 93.75% power reduction.

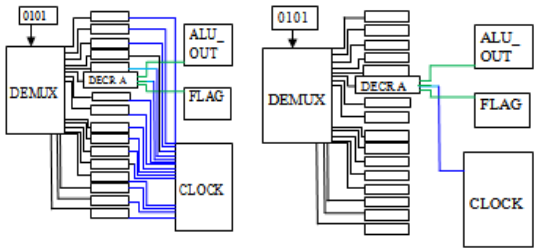

Fig. 11.Without Clock Gate (a), With Clock Gate (b)

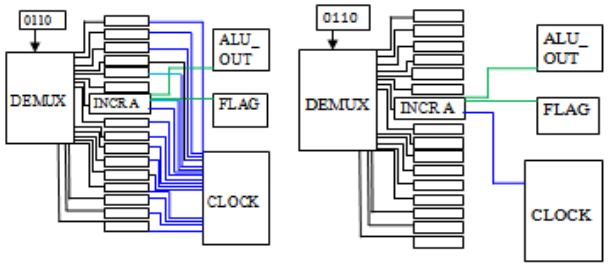

Fig. 12. Without Clock Gate (a), With Clock Gate (b)

G. Increment Data Bus Value

ALU out=A+1; Pass incremented value of A to ALU output. In Clock Gating, we turn off the 15 functional units as shown in Fig12. Hence reduce 93.75% power reduction.

H. Left Shift Data Bus Value

ALU out=A << 1; Left shift A by 1 bit and Pass that value of A to ALU output In Clock Gating, we turn off the 15 functional units as shown in Fig.13. Hence reduce 93.75% power reduction.

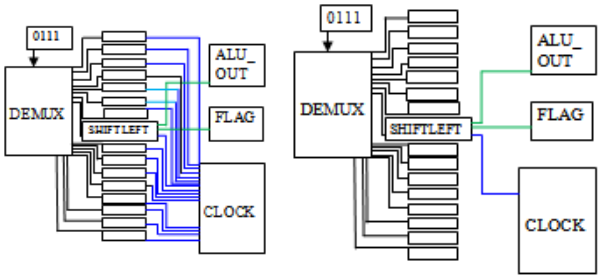

Fig. 13. Without clock gate (a), With clock gate (b)

I. Addition Operation in ALU

ALU out=A+B; Add value of B with value of A and pass to ALU out In Clock Gating, we turn off the 15 functional units as shown in Fig. 14. Hence reduce 93.75% power reduction.

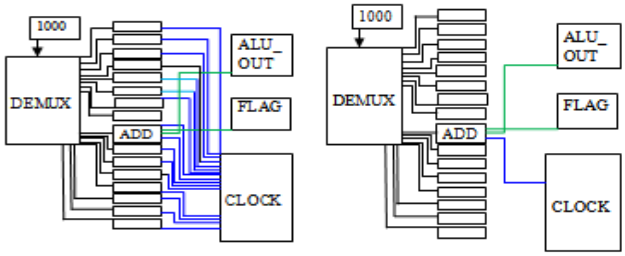

Fig. 14. Without Clock Gate (a), With Clock Gate (b)

J. Subtraction in ALU

ALU out=A-B; Subtract value of B from value of A and pass to ALU out.

In Clock Gating, we turn off the 15 functional units as shown in Fig. 15. Hence reduces 93.75% power reduction.

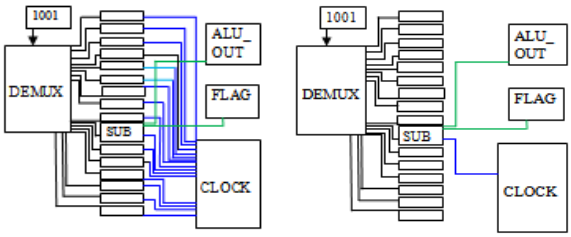

Fig. 15. Without clock Gate (a), With clock gate (b)

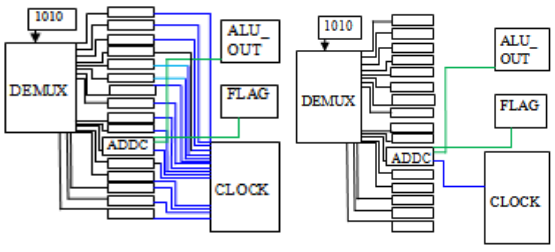

Fig. 16. Without clock gate (a), With clock gate (b)

K. Addition with Carry

ALU out=A+B+Carry_in; Add three values A, B and Carry_in and store that result to ALU out. In Clock Gating, we turn off the 15 functional units other than ADDC as

shown in Fig. 16. Hence reduces 93.75(15/16*100) % power reduction.

L. Subtraction with Carry

ALU out=A-B-Carry in; Subtract value of B from value of A and then subtract Carry In from last result and pass to ALU out. In Clock Gating, we turn off the 15 functional units as shown in Fig. 17. Hence reduce 93.75% power reduction.

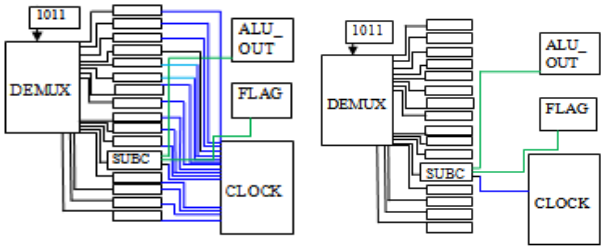

Fig. 17. Without Clock Gate (a), With Clock Gate (b)

M. Logical AND Operation

ALU out=A&B; Calculate Logical A & B and pass that value to ALU outIn Clock Gating, we turn off the 15 functional units as shown in Fig.18. Hence reduce 93.75% power reduction.

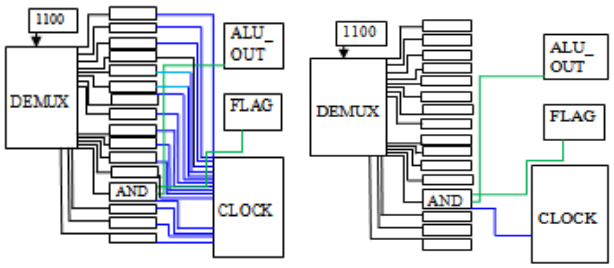

Fig. 18. Without Clock Gate (a), With Clock Gate (b)

N. Logical OR Operation

ALU out=A | B; Calculate Logical A | B and pass that value to ALU out. In Clock Gating, we turn off the 15 functional units as shown in Fig. 19. Hence reduce 93.75% power reduction.

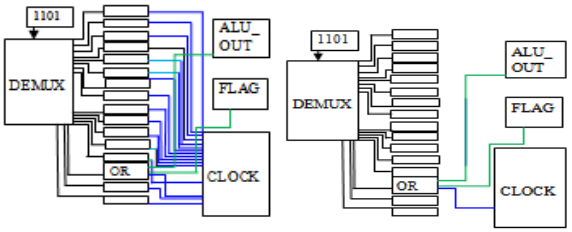

Fig. 19. Without clock gate (a), With clock gate (b)

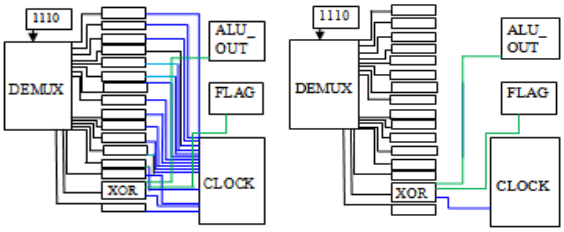

Fig. 20. Without clock gate (a), With clock gate (b)

O. Logical XOR Operation

ALU out=A⊕ B; Calculate Logical A⊕ B and pass that value to ALU out. In Clock Gating, we turn off the 15 functional units as shown in Fig.20. Hence reduce 93.75% power reduction.

P. Logical XNOR Operation

ALU out= (A⊕ B)'; Calculate Logical (A⊕ B)' and pass that value to ALU out. In Clock Gating, we turn off the 15 functional units as shown in Fig.21. Hence reduce 93.75% power reduction.

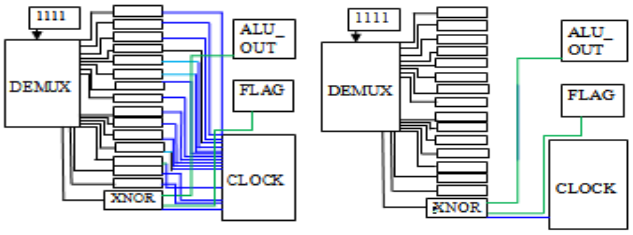

Fig. 21. Without clock gate (a), With clock gate (b)

Q. RTL Technology Schematic

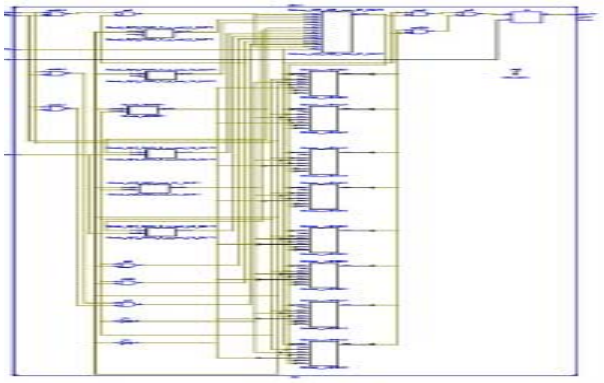

Fig. 22. RTL Schematic of ALU

RTL Schematic generated by Xilinx Synthesis Technology and save with the extension .ngr as shown in Figure: 22. RTL Schematic shows a schematic representation of optimized design in terms of digital logic symbols that are not related to the targeted Xilinx FPGA device.

V. Results

An 8-bit ALU is design and developed for low power processor in the platform Xilinx ISE 14.4 and synthesized on 90nm Spartan-3 FPGA.

ALU Power affected by Clock Frequency:

All Power either dynamic (Clock, Logic, Signal, IOs) is directly proportional to clock Frequency. Power calculation by Xilinx XPower 14.4 is affected with setting of alucg.ncd and alucg.ucf file of Xilinx ISE 14.4.

Frequency	Clock Power	Logic Power	Signal Power	IOs Power
100MHz	2mW	1mW	1mW	0 mW
1000MHz	17 mW	9mW	10 mW	4 mW
10GHz	168 mW	48mW	88 mW	41mW
100GHz	1679mW	153mW	802 mW	410mW
1000GHz	16795mW	1198mW	7983 mW	4099mW

In next phase using clock gating, we turn off rest 15 modules when any module is in execution then theoretical

assumption is 93.75% power reduction. Table II shows 88.23% clock power reduction using latch based clock gating.

TABLE II: LATCH BASED CLOCK GATING

Latch Based Clock Gating	Total Power	Dynamic Power	Clock Power
Without Clock Gate	94mW	41mW	17mW
With Clock Gate	77 mW	25 mW	2mW

Table III shows 70.58% clock power reduction using latch free clock gating.

TABLE III: LATCH FREE BASED CLOCK GATING

Latch Free Based Clock Gating	Total Power	Dynamic Power	Clock Power
Without Clock Gate	94mW	41mW	17mW
With Clock Gate	80 mW	28 mW	5mW

VI. CONCLUSION

Power reduction deals with synthesis, design at circuit level and placement and routing stages, now moved to the System Level and Register Transfer Level. This is possible due to clock gating which always switch off the inactive unit of the design and reduce overall power consumption. The Register Transfer Level approach is always important because hardware designers generally verify power only at the gate level and any changes to the Register Transfer Level needs many design repetition to reduce power. Our designed ALU has 16 functions. Each function has one dedicated module. When one instruction executes in their respective module, others module that was not used by current executing instruction must gated off by the clock gate. From given formula,

$$Power\ \mathrm{Re}duction\% = \frac{Number\ of\ Unit\ Gated}{Total\ Number\ of\ Unit} \times 100$$

Here, when any one of module execute because of clock gating rest 15 modules turned off and hence reduce power (15/16)×100=93.75% power reduction.

VII. FUTURE SCOPE

Clock gating technique is one of the best techniques to reduce dynamic power. There is need to extend clock gating technique to reduce leakage power consumption. Virtex-6 FPGA is based on 40-nm technology. Latest FPGA like Virtex-7, Kintex-7, Artex-7 based on 28-nm technology contribute significant leakage power consumption. There is need to optimize clock gating to reduce leakage power along with dynamic power.

ACKNOWLEDGMENT

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