ALL Digital Phase-Locked Loop (ADPLL): A Survey

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Abstract—**ADPLL is contributing great role in advancement in control system and digital communication since 1980. Design of ADPLL with integrated circuit (IC) techniques has made ADPLL very important component. ADPLL is still continuing to give better results. Now a days ADPLL has great contribution in digital communication systems. This paper gives basic details of an ADPLL. It provides brief summary of the basic ADPLL principle applicable to control systems and digital communication. It also reports components of ADPLL and comparison among them.**

***Index Terms*—DCO, ADPLL, loop filter, phase detector.**

I. Introduction

The PLL is a self-correcting control system in which one signal chases another signal.PLL has four types 1.linear PLL 2.digital phase locked loop 3.all digital phase locked loop 4.software PLL (SPLL).ADPLL takes input as only digital signals. Due to digital signal as input signal so many advantage of the ADPLL exists. In this paper different applications of ADPLL is discussed [1]-[7].

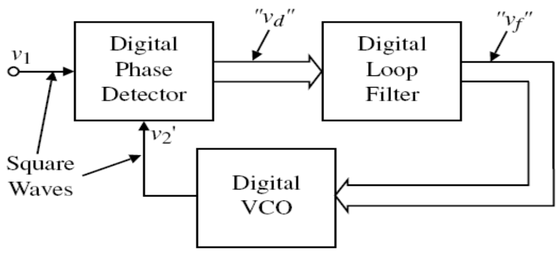

Fig. 1. General block diagram of ADPLL

Beginning of all digital phase-locked loops (ADPLL) started in 1980 [8]. In the 21'st century, researchers has developed a new digitally controlled oscillator (DCO) to obtain good phase and frequency error that was not implemented with 74hc297 IC [1], [8]. In 2005's, a frequency modulated receiving system based on ADPLL was proposed [2] .In 2006's double edge triggered D flip-flop as phase detector was proposed [3] This design reduced 33% of power dissipation. In 2008's digital fm demodulator was proposed [4] It was designed by VHDL. In 2009's frequency modulated modem was implemented on field programmable array (FPGA) [5] In 2010's a field programmable array based linear ADPLL was proposed. This ADDPLL used FPGA for implementation [6] .Recently an all-digital phase-locked loop (ADPLL) having a fault detection of the input reference signal was modeled in Verilog hardware descriptive language (HDL) [7].

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II. ADPLL Design

A. Block Diagram

It contains digital blocks. It uses negative feedback control loop. It takes digital signal only. The signal could be single or combination of parallel digital signals. It consists three blocks: 1.Phase Detector (PD) 2.Loop Filter (LF) and 3.Digitaly Controlled Oscillator (DCO). Fig. 1 gives basic structure of an ADPLL.

The aim of the ADPLL is to interlace the phase input v1 and output v2' and also the frequency. To reduce the difference among two signals PD is used. For removing noise LF is used.

Finally, the digitally-controlled oscillator (DCO) gets the signals from LF and makes closer to the input signal. To realize an ADPLL, existing elements must be digital circuits. There are some advantages: No off-chip components and Insensitive to technology.

B. Phase Detector

It is also called phase comparator. It compares between input and DCO output signal. Output depends upon the phase error. Output signal contains low frequency and higher frequency component. Some of the existing phase detectors are explained below.

1) EXOR gate phase detector

It uses an EXOR logic gate. It compares the reference and DCO signal.

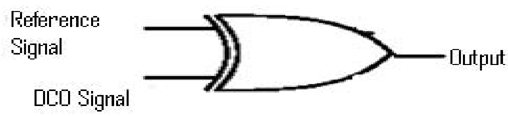


Fig. 2. XOR gate phase detector

Disadvantages of this are it has phase limitation [-90, +90] degrees and it does not sense edges signal edges. Fig. 3 shows the "locked" state [8], [11], [13].

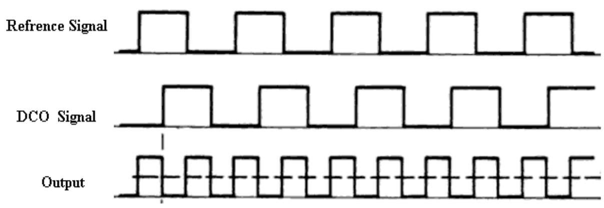


Fig. 3. Waveforms of XOR gate phase detector

2) Edge triggered JK flip-flop phase detector

It contains a JK FF. A phase limitation of this is -180 degrees to +180 degrees. Waveform is shown below [8]-[13].

3) Flip-flop counter phase detector

The phase detector contains a counter and a FF, is shown in Fig. 6. Flip-flop Counter phase detector compares reference and the DCO output signal. In this case FF input S takes input signal and R takes DCO output signal. Output of FF is high when there is error among S and R inputs. Q enables the counter. FF input S resets counter. Output of counter depends upon the phase error. Clock frequency of counter is very high it is M times multiple of input signal is large positive integer [8], [11].Waveform of this is shown below.

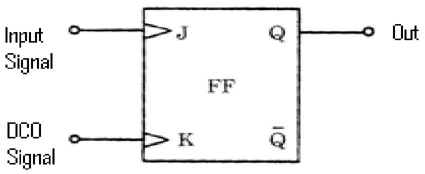


Fig. 4. JK flip-flop phase detector

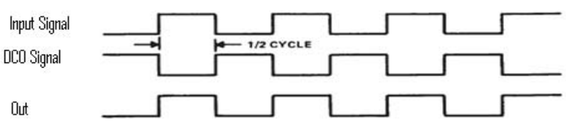
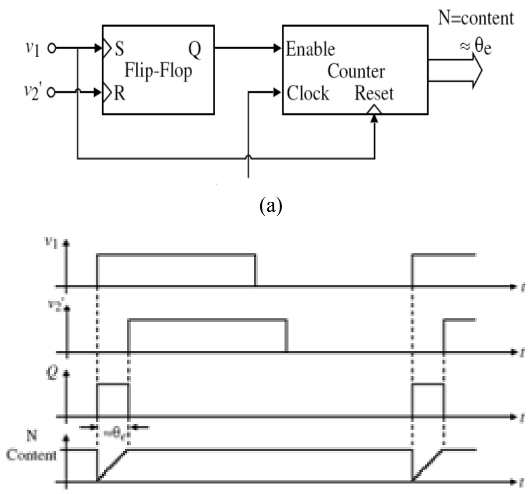


Fig. 5. Waveforms of JK flip-flop phase detector



(a)

(b)

Fig. 6. Flip-flop counters phase detector (a) and corresponding waveforms (b).

4) Phase frequency detector

Phase Frequency Detector (PFD) is very important for an ADPLL .It checks both the signal are in phase .It also checks frequency. A different type of D FF is used .D input is always high. Nor gate takes input as D FF outputs. It resets the FF. For increasing DCO clock signal up signal should high and for decreasing DCO clock signal down signal should high [9].(Fig. 7)

5) Double edge triggered D flip-flops (DETDFF)

DETDFF is based on data selectors is shown Fig.8. For this two FF are used. These two flip-flops are controlled by same CLK. When CLK has logic high, data selectors MUX output port is put through with flip-latch 2.And when CLK has logic low, data selectors MUX output port will is put through with flip-latch1. Hence, whatever states the signals CLK is in, trigger always accepts input signal. Trigger can be changed in both edges of CLK [3].

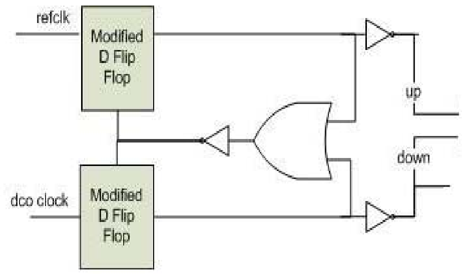


Fig. 7. Phase frequency detector (PFD) is very important for an ADPLL

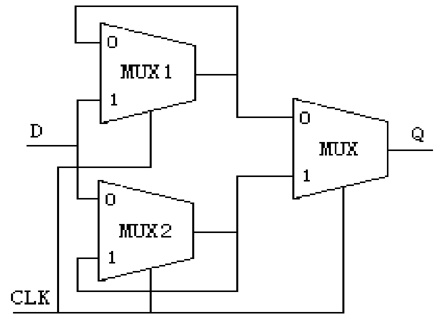


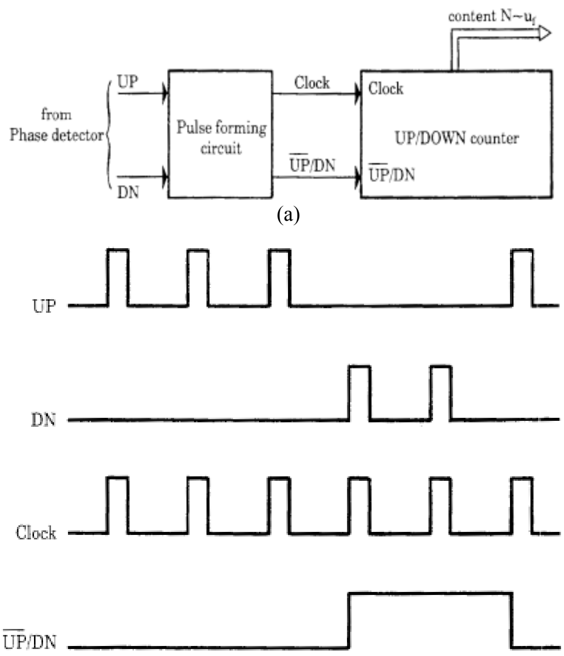
Fig. 8. The Strucure of DETDFF

C. Loop Filter

It is nothing but an integrator. Examples of loop filters are discussed below.

1) UP/down counter loop filter

It is simplest loop filter. It is always operate in conjunction with EXOR or JK FF phase detector. For getting clock and direction signal a pulse forming circuit is used. Counter is incremented on each UP pulses and it is decremented on each down signals .So counter adds both pulses .So its work like an integrator [8], [11].



(a)

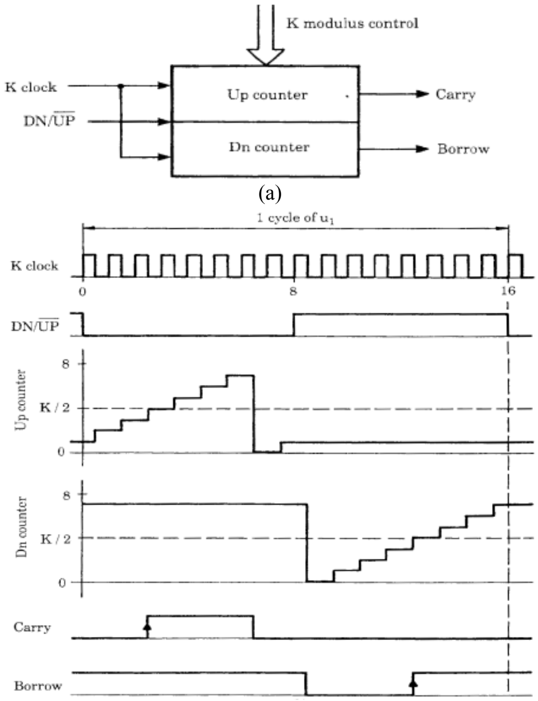
(b)

Fig. 9. Up/down counter loop filter. (a) Block diagram (b) Corresponding waveforms.

2) K counter loop filter

K counter loop filter is very important loop filter .It always works with *JK* or EXOR phase detector. It has two counters .Both are independent .One is called Up and other is Down counter .But both counts in upward direction. Counter has modulus *k*.

So counter contents has range from 0 to *k*-1.Couter clock frequency is M times multiple of center frequency. M has typical values of 8, 16, 32….Down counter is enabled when DN/UP has logic high and up counter is enabled when this logic low value. When contents exceed *k*-1 both counters resets. “Carry” is MSB of the Up counter .The “borrow” signal is MSB of the Down counter. When Up-counter stored data ≥ *k*/2 “carry” is high .When down counter stored data≥ *k*/2 “borrow” is high. Frequency of DCO is controlled by positive edges of the signal [8], [11], [13].



(b)

Fig. 10. K Counter Loop Filter. (a)Block Diagram. (b) Corresponding waveforms.

D. Digitally Controlled Oscillators

Digitally Controlled oscillators are nothing but a modified oscillator .Depending upon output of the loop filter they change their frequency. Some of DCO are explained below.

1) Divide by N counter DCO

A simple ÷N counter works as DCO. High frequency signal operates at very high frequency. Divide by N counter produces N bit parallel output [8], [11]. Drawback of it is we can’t design jitter.

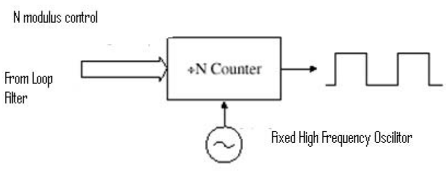


Fig. 11. ÷N Counter DCO

2) Increment-decrement counter

Increment-Decrement Counter consists of two blocks. Carry is assigned to DECR input and Borrow is assigned to INCR input. ID counter with ÷ N counter for again dividing the OUT. Clock of increment-decrement counter is 2N times multiple of center frequency. Fig. 12 gives overall structure [8], [11], [13].

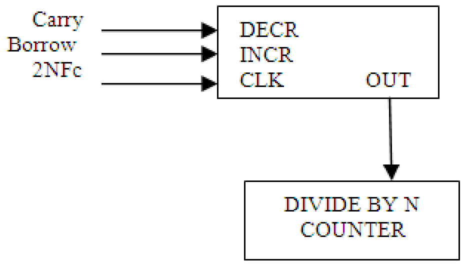


Fig. 12. Increment-decrement counters

If no Carries and Borrows are present then ID counter divides OUT by 2 on the positive edges of ID clock. The logical function for ID counter is given by

ID out = (NOT (1D clock) AND (NOT (togg1e-FF))

If carry is present then half cycle is added and if borrow is present then half cycle is removed from OUT. Here out is output of increment-decrement counter. The adjusted waveform is shown below.

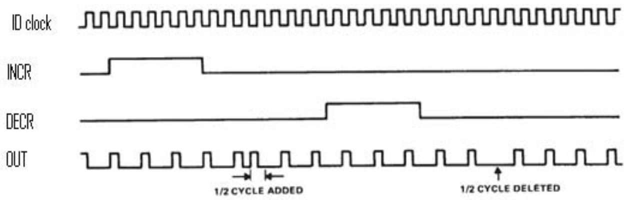


Fig. 13. Waveforms of increment-decrement counter

III. Comparision of Basic Building Block of ADPLL

Tabular from is used for comparing the basic building block of ADPLL. Different implementations of the each block of ADPLL is given in the last.

A. Phase detector

Advantage and disadvantage of various phase detectors are given in Table I. Depending upon advantage and disadvantage of various phase detectors we are selecting our loop filters.

B. Loop Filter

Advantage and disavantage of various loop filters are discussed in the Table II. Depending upon advantage and disadvantage of loop filters we are selecting our digitaly control oscliators(DCO).

C. Digital Controled Osciator

Advantage and disadvantage of various digitaly controled oscliators are discussed in Table III. Depending upon the proper choice of digitaly controled oscliators(DCO) we can avoid ripple problem which is most critcal parametrs while designing the ADPLL .

TABLE I: TYPES OF PHASE DETECTOR AND ITS ADVANTAGES & DISADVANTAGES

Serial No.	Phase Detector		
	Types	**Advantage**	**Disadvantage**
1	EXOR	It produces error pulse on both the edges. Pull in process slow[8].	It is not sensitive to edges.So data might be lost.Phase error lies between -90 to +90 degrees. Smaller phase tracking range[8].
2	JK Flip-Flop	It is sensitive to edges.So no chance of data losses[8].	Phase error lies between -180 to +180 degrees.Larger phase tracking range[8].
3	Flip-Flop Counter	N bit output are possible[11].	Circuit is not simple.It requires three frequency inputs[11].
4	Phase Frequency Detector	Larger phase tracking range.Phase error lies between -360 to 360 degrees. It locks under any condition[8].	Circuit has not simple structure [11].
5	DETDFF	Power disspiation is less and it provides high speed at which it achives a phase-locked state[3] .	Circuit has not simple structure [3].

TABLE II: TYPES OF LOOP FILTER AND ITS ADVANTAGES & DISADVANTAGES

Serial No.	Loop Filter		
	Types	**Advantage**	**Disadvantage**
1.	Up/Down Counter	It is easily adapted to operate in conjunction with an XOR or JK-Flip flop phase detectors and others [11].	It is not perfectly works as a integrator[8].
2.	K Counter	It perfectly works as a integrator[8].	It is not operate with others detectors except XOR or JK-Flip flop[8].

TABLE III: TYPES OF DIGITAL CONTROLLED OSCLLIATOR AND ITS ADVANTAGES & DISADVANTAGES

Serial No.	Digital Controlled Oscillator		
	Types(DCO)	**Advanatage**	**Disadvantage**
1	Divide By N counter	It has simple structure [11].	It does not offer jitter design criterion [11].
2	Increment-Decrement Counter	Good control over Hold range and lock in range [8].	It is not suitable for software implementations[8].

IV. APPLICATIONS OF ADPLL

The use of ADPLL with IC (74HC/HCT297) is developed for digital communications [8], for example, FSK decoder. For wideband frequency tracking and noise reduction ADPLL can be used [12]. PLL heating control system is replaced by ADPLL in 2009 [13]. The developed ADPLL provides simple structure. FM demodulaton an ADPLL circuit was proposed [14]. For mobile phones applications ADPLL is developed [15]. ADPLL is used in high-speed clock generation [16], [17]. There are many ADPLL developed for frequency synthesizers [17]-[19]. In real communication systems like wireless ADPLL is helpful [20]. ADPLL is used in Clock recovery circuit and in frequency synthesizers [21]-[26].

V. CONCLUSIONS

General block diagram of an ADPLL has been discussed.Different types implementations of all the blocks of ADPLL have been presented. Comparision among all the blocks have been reported in detail.Typical applications of the ADPLL is reported. ADPLL block implementations have been presented.

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