Design and Implementation of Image Dithering Engine on a Spartan 3AN FPGA

U. S. Pavitha, S. Nikhila, and H. K. Krutthika

***Abstract*—Digital displays are fast-growing market comprising LCD, plasma, and rear projection television technologies as well as smaller displays for mobile handsets and automobiles, in addition to many other applications. Digital image processing enhances the overall viewing aesthetics of the displayed image and can differentiate the product. Some display devices have color depth less than the color depth of the input data (for example, eight-bit input data and six-bit display color depth). The input data is either truncated or rounded, but this approach usually produces both a loss of detail and may produce large, banded areas of a single color that differs significantly from the original image. Dithering is used to enhance these images.**

***Index Terms*—LCD (liquid crystal display), FPGA (field-programmable gate array).**

I. Introduction

Display hardware, including early computer video adapters and many modern LCDs used in mobile phones and inexpensive digital cameras, show a much smaller color range than more advanced displays. One common application of dithering is to more accurately display graphics containing a greater range of colors than the hardware is capable of showing. For example, dithering might be used in order to display a photographic image containing millions of colors on video hardware that is only capable of showing 256 colors at a time. The 256 available colors would be used to generate a dithered approximation of the original image. Without dithering, the colors in the original image might simply be "rounded off" to the closest available color, resulting in a new image that is a poor representation of the original. Dithering takes advantage of the human eye's tendency to "mix" two colors in close proximity to one another.

Dithering is analogous to the halftone technique used in printing. Dithered images, particularly those with relatively few colors, can often be distinguished by a characteristic graininess, or speckled appearance. For example, a display with only black or white colors can be used to create an image with gray colors by use of dithering (see Fig. 1). The interlaced black and white pixels create the illusion of gray.

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Fig. 1. Illusion of gray color.

Applications of Image Dithering Controllers

- Used in LCD displays
- Used in Color Mobile Handsets
- Used in Video Cameras
- Used in Satellite Camera and receivers
- Medical Imaging Applications
- Defense Imaging Applications
- Other Image processing and display applications

II. Dithering And Display Panel

- The color response time of the LCD is slower and depends on the color content, which presents a challenge in designing an image processing algorithm that can eliminate any viewing artifact. FPGAs offer a critical time-to-market advantage with their design flexibility, allowing designers to re-design the algorithm within the device without having to re-program it.
- Display manufacturers can differentiate from their competitor's products by adding their own proprietary algorithms for true color and motion performance. There are two methods of proprietary video enhancement used for creating a true video performance from a LCD panel.
- The first, a technique called Temporal Dithering, generates a true gray scale for different colors by rapidly switching the pixels between on and off over a certain time period. The second, Spatial Dithering generates the exact amount of color intensity scale. Spatial Dithering can cause spatial noise, or error diffusion, further filtering and fine tuning are required to correct this type of noise.

III. Objective

This project is aimed at design and implementation of Image Dithering Engine based controller on an FPGA. This project work is a block module which needs to be appended with a main module to form a Flat Panel Display Controller. The inputs to this Image dithering controller are given from a precise gamma correction module of a Flat Panel Display Controller. The outputs of this controller are fed to LVDS module to be interfaced to a Flat panel display. Commercially available flat panel display controllers (ASICs) cannot be reprogrammed. But this project work involves the design of Image dithering controller on FPGA which can be reprogrammed to meet different specification requirements.

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The programming of the logic has been done on to Spartan 3AN FPGA, which is the latest and robust programmable IC available in the market.

A. Display Panel

The display solution FPGA consists of a DVI Input interface, Color Temperature Correction, Precise Gamma Correction, an Image Dithering Engine, and Low-Voltage Differential Signaling (LVDS) Transmit (TX) or DVI TX output interface (see Fig. 2).

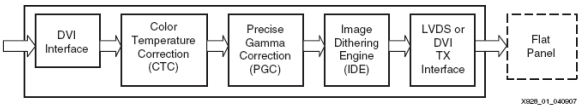

Fig. 2. Display panel design flow.

TABLE I: BLOCK DESCRIPTION OF DISPLAY PANEL.

Block Name	Block Description
DVI Receiver	Accepts input video in DVI format
Color Temperature Correction (CTC)	Incoming RGB values of the entire frame are corrected to the user set color temperature
Precise Gamma Correction (PGC)	Accepts the pixel stream, processes it as per the required gamma value and sends the modified pixel stream out to the next processing module
Image Dithering Engine (IDE)	Receives the 3x10 bit gamma corrected pixel stream from the precise gamma correction module and dithers it to 3x8 bit pixel stream, without , losing the video quality
Display Interface	Allows the DVI transmitter to directly drive LCD modules with LVDS interfaces

B. Display Colours

A typical observer can distinguish between a dozen to three dozen distinct grey levels or intensity variations. When color is added, then a typical observer can discern thousands of color shades and intensities. Also, color plays a very important role in image analysis when used as a descriptor. A full color image, also known as a True Color image, has three different bands (R=red, G=green, B=blue), one per color.

C. Colour Models

A color model is a 3D unique representation of a color. There are different color models and the use of one over the other is problem oriented. For instance, the color model RGB is used in hardware applications like PC monitors, cameras and scanners, the CMY color model is used in color printers, and the YIQ model in television broadcast.

An RGB image and its data structure are as shown in the Fig. 2. Each pixel has three components: Red, Green and Blue components, which added together, can generate most of the existent colors. Each color can be a point in the RGB color model cube. Red, Green and Blue are known as the primary colors.

These colors can be added to produce secondary colors which are:

- Magenta =Red + Blue
- Cyan = Green +Blue
- Yellow = Red + Green

Fig. 3. RGB image.

The RGB color model is an additive color model in which red, green, and blue light are added together in various ways to reproduce a broad array of colors. The name of the model comes from the initials of the three additive primary colors, red, green, and blue.

RGB is a device dependent color space different devices detect or reproduce a given RGB value differently, since the color elements (such as phosphors or dyes) and their response to the individual R, G, and B levels vary from manufacturer to manufacturer, or even in the same device over time. Thus an RGB value does not define the same color across devices without some kind of color management.

IV. THE 24BIT RGB REPRESENTATION

In the 24-bit RGB representation of the true color, color values for each pixel encoded in a 24 bits per pixel fashion in which three 8-bit unsigned integer (0 through 255) represent the intensities of red, green, and blue. The following image shows the three “fully saturated” faces of a 24-bit per pixel RGB cube, unfolded into a plane.

- (0, 0, 0) is Black
- (255, 255, 255) is White
- (255, 0, 0) is Red
- (0, 255, 0) is Green
- (0, 0, 255) is Blue
- (255, 255, 0) is Yellow
- (0, 255, 255) is Cyan
- (255, 0, 255) is Magenta

A. Dithering Algorithms

There are several algorithms designed to perform Dithering

- One of the earliest, and still one of the most popular, is the Floyed-steinberg Dithering algorithm, developed in 1975.
- One of the strengths of this algorithm is that it minimizes visual artifacts through an error diffusion process; error diffusion algorithms typically produce images that more closely represent the original than simpler dithering algorithms.

The main characteristics of the Dithering algorithm are:

- Black maps to black.
- White maps to white.

- The average value of a group of dithered pixels approximates the average of the original color values.
- Dots spaced as far apart as possible.

B. Dithering Classification

- Spatial dithering
- Tempo spatial dithering
- Random dithering

Spatial Dithering: In some cases a digital display may not be able to generate all of the required (or desired) intensity levels. For example, in an 8-bit digital intensity scale, there may be duplicates or gaps in some of the 256 levels produced by the display device. (This is sometimes an issue over only a portion of the gray scale as the result of an irregular transfer characteristic for the display device typical for LCD and LCoS technologies). To overcome this limitation, the display electronics is configured to automatically adjust the intensities of neighboring pixels so that their combined intensities average out to the desired values. This procedure is called Spatial Dithering and it increases the gray-scale resolution. Image sharpness is reduced somewhat in return for a smoother gray-scale and reduced intensity contouring. Spatial dithering is used in most plasma and DLP displays and in some LCDs, but never in CRTs, because they already produce a perfectly smooth intensity scale. The technique typically provides an additional 2-bit of intensity resolution.

The averaging process may involve only adjacent pixels, or it can encompass larger groupings of nearby pixels to produce a finer intensity scale. The dithering process introduces a form of spatial noise into the image. The dithering algorithm may involve fixed pixel pattern, which is often more noticeable because it tends to produce repeating pixel patterns on the screen, or error diffusion. This generates a seemingly random pattern and a finer intensity scale, but also introduces more random noise into the image. In some cases displays will provide a menu option to choose among several dithering algorithms. Spatial Dithering is also called Digital half toning.

Temporal Dithering: The use of dynamically controllable displays such as CRT's and flat panel displays has created a new opportunity for the improvement of halftones through the use of temporal dithering. Temporal dithering refers to the rendition of a desired gray level with a spatial distribution of flickering pixels.

Temporal Dithering or Frame-Rate Control (FRC) or Dynamic Dithering looks like quickly moving patterns. Many monitors cannot make small brightness steps, especially in the darker shades. Instead, they rapidly alternate between darker and brighter shades for the individual pixels, such that at least on average the brightness is correct.

Also, most TN panels represent colors using only 6 bits per RGB color, or 18 bit in total, and are unable to display the 16.7 million color shades (24-bit true color) that are available from graphics cards. Instead, these panels display interpolated 24-bit color using a dithering method that combines adjacent pixels to simulate the desired shade. They can also use a form of temporal dithering called Frame Rate Control (FRC), which cycles between different shades with each new frame to simulate an intermediate shade. Such 18 bit panels with dithering are sometimes advertised as having "16.2 million colors". These color simulation methods are noticeable to many people and highly bothersome to some.

FRC tends to be most noticeable in darker tones, while dithering appears to make the individual pixels of the LCD visible. Overall, color reproduction and linearity on TN panels is poor. Short comings in display color gamut (often referred to as a percentage of the NTSC 1953 color gamut) are also due to backlighting technology. It is not uncommon for displays with CCFL (Cold Cathode Fluorescent Lamps)-based lighting to range from 10% to 26% of the NTSC color gamut, whereas other kind of displays, utilizing RGB LED backlights, may extend past 100% of the NTSC color gamut, a difference quite perceivable by the human eye.

Random Dithering: Random Dithering is a method of dithering which produces monochrome (black and white) images. Random Dithering works by choosing a different random value for each pixel in the image. If the p pixel is more intense (usually a higher number) than the random value, it becomes white, if not, it becomes black.

Random Dithering tends to produce images with a lot of high frequency noise artifacts (like a badly tuned TV picture), and so is usually not appropriate unless you actually wish to achieve this special effect. However, there are a few cases (generally very simple images with little detail - such as a picture containing a smooth gradient of grays from black to white), where random dithering may actual produce better results than other methods. Generate a random number from 0 to 255. If it is greater than the pixel value at that point, plot the white pixel, else black pixel. It is useful in reproducing very low frequency images.

V. The Design And Modeling

The algorithm achieves Dithering by diffusing the color of a pixel to its neighboring pixels, according to the distribution. By alternating each pixel's color value rapidly between two approximate colors in the panel's color space display panel which natively supports 18-bit "true" color image (8 bits per channel).

A. Functional Description of Image Dithering Engine (one color shown)

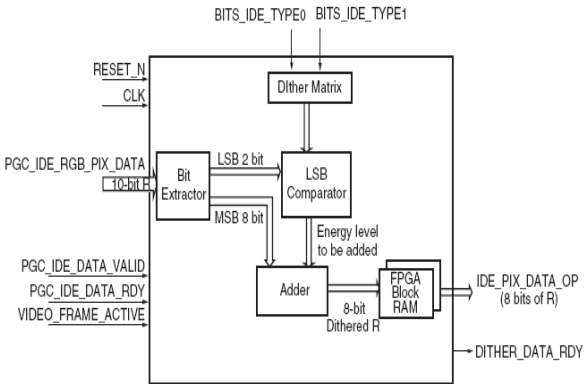

Fig. 4. Functional description of IDE (for one color).

The Fig. 4 shows, the functional description of image dithering engine for one color and same holds good for remaining colors such as green and blue where the pixels are extracted from the bit extractor and undergoes dithering

depending upon the conditions and finally the 8 bits from each color are fed to LVDS module when DITHER_DATA_RDY signal is high.

B. Signal Description of the IDE Module

TABLE II: SIGNAL DESCRIPTION OF IDE MODULE.

Port Name	I/O	Detailed Description
RESET_N	1	This input is asserted Low to reset the IDE module.
CLK	1	The digital clock manager (DCM) generates the system clock.
BITS_IDE_TYPEO	1	Dither type election for encoding.
BITS_IDE_TYPE1	1	Dither type selection for encoding.
PGC_IDE_DATA_VALID	1	The PGC module asserts this signal to the IDE module to indicate the input signal data is valid. This signal is held asserted for the entire line duration.
PGC_IDE_DATA_RDY	1	The PGC module generates a pulse on this signal to the IDE module when gamma corrected data is available.
PGC_IDE_RGB_PIX_DATA[29:0]	1	The PGC module places -bit R,G and B gamma corrected pixel data on this bus for the IDE module.
VIDEO_FRAME_ACTIVE	1	This signal is asserted High ti indicate a valid frame. It goes Low when the frame ends.
IDE_PIX_DATA_OP[23:0]	0	This output bus provides the dithered 8-bit RGB values.
DITHER_DATA_RDY	0	This signal is asserted to indicate dithered data is available.

VI. IMAGE DITHERING ALGORITHM DESCRIPTION (IDE)

The IDE module receives 30-bit (10 bits of data ×3 for R'G'B') pixel streams from the Precise Gamma Correction (PGC) module. The image dithering engine operates only on the active pixels. It uses a spatial dithering technique with a 2 ×2 dithering matrix for 10- to 8-bit dithering.

When a 3×10 bit data stream comes in, for example, the two least significant bits (LSBs) of the three R, G, and B colors contain the most "fine" color information and are selected away from the eight remaining MSB bits. The two LSB truncated bits effectively are an "error." These two bits can have any value from 00 to 11 (binary) providing four finer color levels (0%, 25%, 50%, and 75%) to the remaining eight bits. This error is spread over adjacent pixels.

The following example shows the weights in the 2×2 matrix:

0 1
2 3

The following example shows how the above weight table is spread across the display space.

0 1 0 1 .....
2 3 2 3 .....
0 1 0 1 .....
2 3 2 3 .....
. . . .

When dithering with the least significant two bits of input data, the IDE uses spatial, tempo-spatial, and random spatial dithering with 2×2 pixel blocks. When complete, the 24-bit dithered data (eight bits for each R, G, and B) are sent to the LVDS/DVI TX interface along with a dither_data_ready signal.

VII. INPUTS AND OUTPUT FORMATS

Image Dithering Engine Receives the 3×10-bit gamma corrected pixel stream from the precise gamma correction module and dithers it to 3×8-bit pixel stream, without losing the video quality.

VIII. CONCLUSION

The project work is successfully carried to implement IDE controller on a Spartan 3AN FPGA. The specifications for the IDE controller are met. The inputs for this controller can be from a PGC block inside the Flat Panel Display controller. The Outputs can be applied on to a LVDS module and then connected to Flat Panel Displays. The design was started from scratch with just specifications in hand. To carry out the different implementation methodologies like Synthesis, Floor planning, Place and route and programming Xilinx ISE is used. The results have been successfully tested and using Chip scope Pro software.

IX. FUTURE WORK AND ENHANCEMENT

- At present the IDE controller is capable of producing 8-bits of pixel data, which can be applied as inputs to a LVDS module. The present and future display technologies are operational with 32-bit pixel values. The same IDE controller can be enhanced to produce 32-bits of R, G and B pixel information, which will enhance the quality of the picture.
- At present, the design has been implemented using Spartan 3AN FPGA (To use the chip scope capability). The design can be further enhanced and optimized to be implemented on cheaper FPGAs/CPLDs to go into the market at cheaper cost.
- The same design can be taken for ASIC flow and the chip can be Mass-Manufactured to produce the chip to the market at lower cost and higher profit.

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