Design of Low Power ASK CMOS Demodulator Circuits for passive Ultra High Frequency Tag

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***Abstract*—This paper presents a low-power, passive, UHF RFID tag design. In order to reduce its cost, diode- connected NMOS in a standard CMOS technology is used instead of Schottky diodes. Here low power Amplitude Shift Keying (ASK) demodulator of Radio Frequency Identification (RFID) tag module is designed. RFID tag is pursued the least area, low price and low power. Here we used ASK demodulator, designed without resistors and capacitors. It uses a minimum of MOSFTES for designing envelope detector and Schmitt-trigger and it is differing from the existing ASK demodulator. This type of ASK demodulator is efficient in terms of, power consumption, and layout.**

***Index Terms*—ASK demodulator, RFID tag, ASK demodulation, envelope detector, Ultrahigh Frequency**

I. Introduction

Passive UHF RFID distinguishes itself from others in the near field item-level tagging applications, mainly due to its high data rates, small antenna sizes and low costs. To lower the tag cost for wide applications, such as supply chain management, chip area for tags is one of the crucial considerations. Apart from its cost, low power consumption is also required for passive UHF RFID, not only due to the passive working principles, but also for a longer operating range in the order of several meters or even longer. As the RF signal power decreases rapidly with its communication distance, the induced voltage across the antenna is quite small, typically in the order of 200mV. This means micro-power rectifier has to function properly with such low input voltages. Moreover, the voltage reference following the rectifier needs to be optimized for low voltage operation to reduce the burden on the rectifier. Fig. 1 shows the diagram of the proposed tag IC. The rectifier, regulator, demodulator, modulator, clock generator and the baseband processor are all integrated into the tag IC and put onto the same chip. The rectifier, using low threshold voltage, triple-well NMOS to reduce the required minimum input voltage, will be proposed in Section II. The self-biased, resistor-less band gap voltage reference using mutual compensation, which achieves sub-1V operation with low temperature coefficient, will be presented in the III. The clock generator together with ASK modulator and discuss the design of the baseband processor using energy aware, irregular clock structure together with clock gating to achieve good power saving.

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II. Rectifier

The rectifier converts the input AC voltage into DC voltage, which is further regulated by the voltage regulator to provide power supply to the circuits in the tag. The single stage structure and the simplified circuit diagram for the CMOS rectifier are shown in Fig. 2a and Fig. 2b, respectively. Low threshold-voltage NMOSFET is chosen to minimize the conduction loss of the rectifier. Compared with the case using Schottky diodes, the utilized approach saves the fabrication cost for extra masks the Schottky diode needs. A 16-stage rectifier is designed to generate an output Voltage of 1.3V from the worst-case of input peak-to-peak. Voltage of 180mV under the condition of 50ohm input impedance.

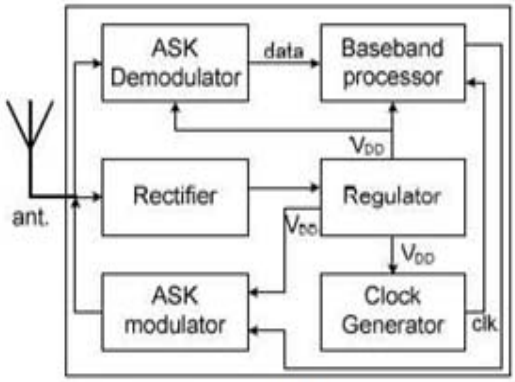

Fig. 1. Passive UHF RFID tag diagram

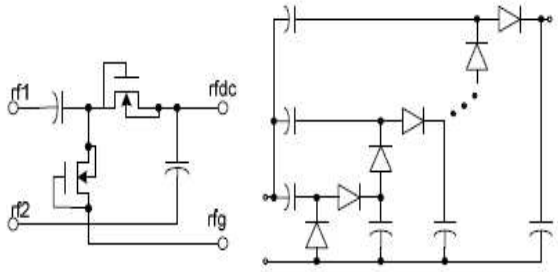

Fig. 1. (a). Single stage structure (b): Circuit of Rectifier

The minimum input power entering the rectifier is -7.6dBm, and the optimum area for the rectifier is 1200µm x600µm.

When input amplitudes are low, a single rectifier stage does not usually produce high enough DC output voltage VL. A number of rectifier stages can be cascaded in a charge pump-like topology to increase VL. The RF inputs are fed in parallel into each stage through pump capacitors CP, and the DC outputs add up in series to produce VL. Each stage contains rectifying elements like transistors and/or diodes. Increasing the number of stages decreases Vto. Thus there is usually an optimum number of stages for

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a given topology minimizes the rectifier OM.

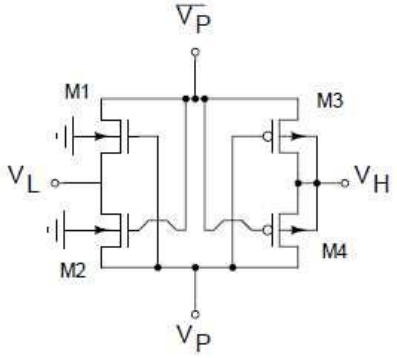

Fig. 2. Voltage regulator

III. Baseband Processor

One of the constraints in the baseband processor design is the limited power consumption under low supply voltage. Another constraint is the weak wireless input from the RFID reader. The input is prone to interference and data integrity is a critical issue in the processor design [9]-[11]. Moreover, the input is in a serial, PIE format. Thus, the throughput of the processor is limited. The block diagram of the proposed baseband processor is shown in Fig. 3. The data flow of the processor is based on the "input-verify-respond" steps. Input PIE_LEN_COUNTER is the extracted time value from the Demodulator.

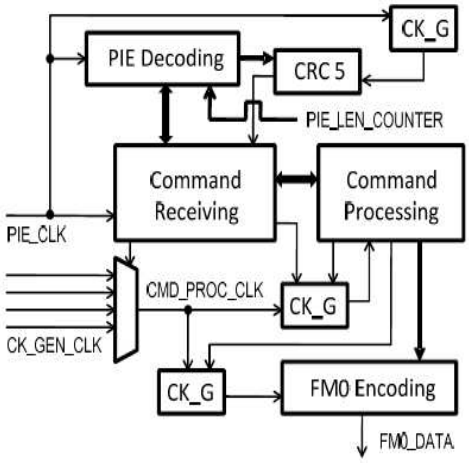

Fig. 3. Baseband processor

In this PIE Decoding block, the preamble, frame and PIE data embedded in the input is identified and decoded. When error is detected, the whole circuit goes back to the ready state.

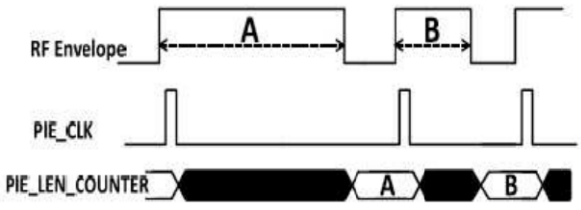

Fig. 4. Timing step with irregular clock

In order to increase the efficiency of the baseband processor, reception and verification of the input data is implemented in a pipelined manner. To achieve good power saving, an energy-aware, irregular clock is used in this design. As shown in Fig.4, the conventional command handler is partitioned into two parts. One part, including the PIE Decoding block and the Command Receiving block, is triggered by an irregular clock, PIE_CLK. The remaining part, the Command Processing block, is triggered by a regular clock, CMD_PROC_CLK. As shown in Fig3, pulses with width of 20ns in the irregular clock, PIE_CLK, are synchronized by the rising edges in the envelope of the RF signal. Because the energy supply is abundant after the rising edge of the RF envelope, the clock can easily trigger the PIE Decoding block and Command Receiving block without any interruption in the power supply. The regular clock, CMD_PROC_CLK, comes from the ring oscillator outputs. Its frequency (62.5 kHz ~ 500 kHz) is equal to the link frequency for the backscattering signal, FM0_DATA. To reduce dynamic power dissipation, Clock Gating blocks (CK_G) are added into the design to stop the propagation of the clocks when the blocks are in the idle state.

ASK DEMODULATOR

To save power and simplify the compensation of the LDO converter, a single stage amplifier is adopted to drive the power PMOSFET directly. The NMOSFET input transistors work in sub-threshold region for low-voltage (sub-1V) and low-power operation. A 1-nF MOS capacitor is used to store sufficient charge to power up the tag when there is very little or even no RF power available to the chip during backscattering. The simulated load transient response of the

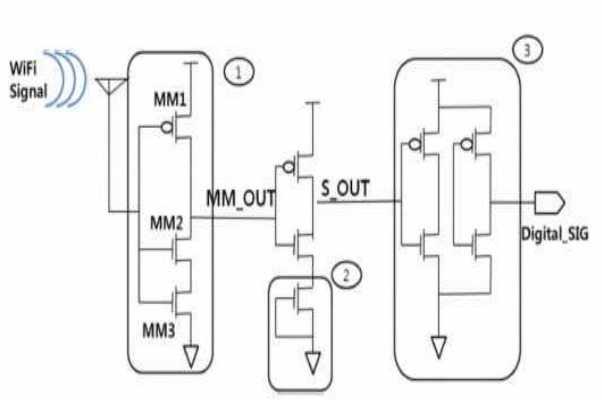

Fig. 3. ASK demodulator circuit

Voltage regulator is shown in Fig. 5. The proposed regulator can recover within 3 μs with only 1mV voltage spike when the loading current changes from 1μA to 10μA. Moreover, it can also work well under 50μA load transient change. To save chip area, seven PMOS transistors with substrate connected to the source terminal are used as a potential.

IV. Conclusion

The UHF RFID tag design consumes low power, occupies less area ant it is cost effective. In order to reduce its cost, diode-connected NMOS in a standard CMOS technology is used instead of Schottky diodes. ASK demodulator does not uses resistors and capacitors in its implementation, so it is structurally very simple and it consumes low power. This proposed ASK demodulator will

contribute miniaturization and low power consumption of RFID tag

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